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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,231	07/24/2001	Jack Regula	136.1005.01	4335

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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/912,231	REGULA ET AL.	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/21/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to the communication filed 4/12/04. Currently claims 1-38 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Information Disclosure Statement

Applicant's IDS, received 10/21/02, was previously considered by Examiner but may not have been sent in the previous Office Action. An additional copy is being sent in this Office Action.

Claim Rejections - 35 USC § 102

Claims 1-16, 19-35, and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Carey (US 6460174).

Regarding claims 1 and 38, Carey discloses an on-chip communication bus and a plurality of stations that couple on-chip components to the bus (e.g., col. 2, lines 33-36), where each station has a dedicated track which it can use to send information to other stations (e.g., col. 2, lines 29-30).

Regarding claim 2, Carey also discloses packet based communication (e.g., col. 4, lines 40-42).

Regarding claim 3, Carey also discloses an inter-integrated circuit component (e.g., col. 2, lines 36-39).

Regarding claim 4, Carey also discloses an initiator that requests permission to transmit outgoing data over a track to another station and that transmits the outgoing data (e.g., col. 5, lines 1-4), an arbiter that evaluates requests and selects a track (e.g., col. 2, lines 52-57), and a target that receives the incoming data (e.g., col. 2, line 40).

Regarding claim 5, Carey also discloses a grant multiplexor for selecting a grant line (e.g., col. 2, lines 52-55).

Regarding claim 6, Carey also discloses plural smaller multiplexors distributed across the chip (e.g., col. 2, lines 53-54, "more requests").

Regarding claim 7, Carey also discloses the arbiter connected a track multiplexor for selecting a track (e.g., col. 2, lines 52-55).

Regarding claim 8, Carey also discloses plural smaller multiplexors distributed (e.g., col. 2, lines 53-54, "more requests").

Regarding claim 9, Carey also discloses a source queue (e.g., Figure 2, "22").

Regarding claim 10, Carey also discloses a first-in-first-out register (e.g., col. 11, line 61).

Regarding claim 11, Carey also discloses a destination queue for incoming data (e.g., Figure 4, "28").

Regarding claim 12, Carey also discloses a first-in-first-out register (e.g., col. 14, line 1).

Regarding claim 13, Carey also discloses a source queue and destination queue (e.g., Figure 2, "22", Figure 4, "28").

Regarding claim 14, Carey also discloses the source and destination queues serve to separate a first clock domain for the on-chip communication bus from a second clock domain for one of the plurality of on-chip components (e.g., col. 13, lines 64-67, col. 14, lines 8-9).

Regarding claim 15, Carey also discloses more than on component coupled to the bus through one of the stations (e.g., col. 2, lines 36-39).

Regarding claim 16, Carey also discloses smaller multiplexors distributed (e.g., col. 12, lines 3-4), pipeline storage elements to maintain transmission speed (e.g., col. 9, lines 37-41).

Regarding claim 19, Carey discloses a method of communicating between a plurality of stations coupled to on-chip components, and communicating between stations using an on-chip communication bus (e.g., col. 2, lines 33-36), where each station has a dedicated track which it can use to send information to other stations (e.g., col. 2, lines 29-30).

Regarding claim 20, Carey also discloses packet based communication (e.g., col. 4, lines 40-42).

Regarding claim 21, Carey also discloses an inter-integrated circuit component (e.g., col. 2, lines 36-39).

Regarding claim 22, Carey also discloses sending a request from a first station to a second station, evaluating the request and sending a grant signal (e.g., col. 5, lines 1-4), selecting a track (e.g., col. 2, lines 52-57), sending and receiving the data at the second station (e.g., col. 2, line 40).

Regarding claim 23, Carey also discloses sending the request is performed by an initiator, evaluating is performed by an arbiter at the second station, selecting the track is performed by the arbiter at the second station (e.g., col. 5, lines 1-4), sending the data or command is performed by the initiator and receiving the data is performed by a target at the second station (e.g., col. 2, line 40).

Regarding claim 24, Carey also discloses a grant multiplexor for selecting a grant line (e.g., col. 2, lines 52-55).

Regarding claim 25, Carey also discloses plural smaller multiplexors distributed across the chip (e.g., col. 2, lines 53-54, "more requests").

Regarding claim 26, Carey also discloses the arbiter connected a track multiplexor for selecting a track (e.g., col. 2, lines 52-55).

Regarding claim 27, Carey also discloses plural smaller multiplexors distributed (e.g., col. 2, lines 53-54, "more requests").

Regarding claim 28, Carey also discloses a source queue (e.g., Figure 2, "22").

Regarding claim 29, Carey also discloses a first-in-first out register (e.g., col. 11, line 61).

Regarding claim 30, Carey also discloses a destination queue for incoming data (e.g., Figure 4, "28").

Regarding claim 31, Carey also discloses a first-in-first out register (e.g., col. 14, line 1).

Regarding claim 32, Carey also discloses a source queue and destination queue (e.g., Figure 2, "22", Figure 4, "28").

Regarding claim 33, Carey also discloses the source and destination queues serve to separate a first clock domain for the on-chip communication bus from a second clock domain for one of the plurality of on-chip components (e.g., col. 13, lines 64-67, col. 14, lines 8-9).

Regarding claim 34, Carey also discloses more than on component coupled to the bus through one of the stations (e.g., col. 2, lines 36-39).

Regarding claim 35, Carey also discloses smaller multiplexors distributed (e.g., col. 12, lines 3-4), pipeline storage elements to maintain transmission speed (e.g., col. 9, lines 37-41).

Claim Rejections - 35 USC § 103

Claims 17-18 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carey as applied above in claims 1 and 19, respectively, in view of Adams (US 2001/0042147).

Regarding claims 17 and 36, Carey fails to disclose a watchdog at each station; however, this watchdog circuit is disclosed by Adams. Adams discloses a watchdog circuit that determines if its station has gone offline (e.g., paragraphs 64-65). It would have been obvious to combine Adams with Carey because

Adams discloses an improvement for a system such as Carey of a data router for stations, and teaches the advantage of using a watchdog circuit when a station is busy. Therefore it would have been obvious to one of ordinary skill in the art to combine Adams with Carey at the time the invention was made.

Regarding claims 18 and 37, Carey does not disclose this, but Adams does. Adams discloses that if the station has gone offline that watchdog circuit informs a controller connected to the system (e.g., paragraphs 64-65).

Response to Arguments

Applicant's arguments filed 4/12/04 regarding the 102 rejection using Carey against all but claims 17 and 36, have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that Carey "does not teach that each module has a dedicated track within the routing network 4. Presence of dedicated connections by itself does not require each module to have a dedicated track" (p. 13). Examiner maintains that Carey teaches a dedicated path as the citation shows; therefore, the issue is the meaning of the term "track". In the specification, Applicant states: "According to the invention, on-chip communication bus 12 includes plural tracks. These plural tracks allow more than one component to communicate with another component simultaneously. Each track preferably includes lines for data bits and other control information. For example, one embodiment of a track includes lines for 64 bits of data, eight

command/byte enable (C/BE) signals, two parity signals (one per double word of data), a start of packet signal, and an end of packet signal" (pp. 9-10). From this description of a track, it is reasonable to broadly conclude that a track is essentially a bus, albeit a bus with point to point, that is, dedicated, communication. From this description, there is no sense of any feature that distinguishes from such a characterization, nor can any distinction be seen in Carey's disclosure of a dedicated bus.

Thus the rejection of claim 1 is maintained.

Regarding claims 3 and 21, Applicant argues that Carey fails to teach an "inter-integrated-circuit" component as claimed. Applicant argues for a specific, narrow interpretation of the terminology as referring specifically to a standard bus "developed by Philips Semiconductors in the early 1980s" (p. 13). Such an interpretation is consistent with the introduction of the term in the specification, where "inter-integrated terminology" is introduced (p. 8); therefore Examiner accepts this precise meaning of the term. As currently claimed however, this feature is among those listed in the alternative and therefore it is not necessary for the prior art to disclose each and every term claimed in the alternative.

Thus the rejection of claims 3 and 21 is maintained.

Regarding claim 4, Applicant argues that Carey where cited "describes that the 'central control logic arbitrates between the requests of the initiator ports 8 to determine which one or more requests are allowed onto the distributed routing network.' Carey, col. 2, lines 52-54. Note that the central control logic is depicted as separate from the modules 6. Carey, Figure 1. Thus, Carey

apparently does not disclose a station or module that includes an arbiter that selects a track" (p. 14). It is true that the arbitration is centrally located, but a closer look at the control logic is necessary to determine whether an arbiter is assigned to each station, particularly in the event of dedicated bus lines. In providing details of the arbiter, Carey discloses: "The arbiter 38 makes an arbitration decision based on each packet of information. The arbiter uses the following information to make the arbitration decision: the initiator making the request; the number of outstanding requests (via input 120) (this is optional); the availability of the target (via input 122); the arbiter makes a decision once per packet; and the arbitration method (defined by input 118)" (col. 13, lines 1-10). From this disclosure it can be determined that if the target is available for arbitration, then arbitration is done; specifically, "an arbiter that evaluates requests from other stations and selects a track on which to receive incoming data" as claimed, is disclosed.

Thus the rejection of claim 4 is maintained.

Regarding claims 15 and 34, Applicant argues that Carey "does not teach that multiple components are connected to the bus using the same station, i.e., using the same port to the bus" (p. 14). In claim 1, the "on-chip components" are recited as "coupled" to the "communication bus" by stations (i.e., "stations that couple a plurality of on-chip components to the on-chip communication bus"), while claim 15 further limits, that more than one component is coupled through one station. What constitutes a component is not recited, which thusly requires a broad interpretation on the part of the Examiner. Components are "coupled"—

from this one might reasonably interpret a component as some item that is addressable beyond the addressing of the port itself. To determine whether Carey discloses some equivalent, one is led to consider any specific details of the transmitted communication. In the instant case, one finds Carey discloses: "The first 8 bits A are used by the request transport to identify the target and thus route the packet. The remaining 24 bits B, which are sometimes referred to as the address, are used by the target port to *identify a location within the associated module* or a function of that module. The second 24 bits B are not used by the request transport in order to route the packet" (col. 4, lines 40-49, emphasis added). It seems clear that Carey addresses "components" through or beyond the port. This is deemed to be a reasonable interpretation of the claim language and one anticipated by Carey.

Thus the rejection of claims 15 and 34 is maintained.

Applicant's arguments, with respect to the 112 and 101 rejections, have been fully considered and are persuasive.

Applicant's arguments, with respect to the 102 rejection using Carey of claim(s) 17 and 36 under 102, have been fully considered and are persuasive. Applicant's arguments, with respect to the 102 and 103 rejections using Apostol as base and teaching reference, respectively, have been fully considered and are persuasive. Therefore, these rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Adams.

Regarding claims 17 and 36, Applicant argues that "Carey does not teach the use of a watchdog timer in the cited text or, it appears, elsewhere." (p. 15). Applicant argues for a particular meaning to the term watchdog as performing "a specific operations after a certain period of time if something goes wrong with an electronic system and the system does not recover on its own" (p. 15, quoting an online dictionary). Applicant enables this in the specification (p. 24): "If a station stalls or goes offline for more than the predetermined amount of time, that station's watchdog timer can inform a controller for the communication system...." Examiner concurs that any interpretation using Carey is inconsistent with Applicant's use of watchdog. Therefore the 102 rejection of claims 17 and 36 using Carey is withdrawn.

Regarding use of Apostol in 102 and 103 rejections, Examiner agrees with Applicant that Apostol's claim to provisional priority is improper. These rejections have been withdrawn. A new rejection of claims 17-18 and 36-37 using a different teaching reference is presented supra; hence this Office Action is non-final.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The

fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

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